

Title (en)  
Multilayer type chip inductor

Title (de)  
Mehrschichtige Chip-Induktivität

Title (fr)  
Inductance de puce multicouche

Publication  
**EP 1011115 A1 20000621 (EN)**

Application  
**EP 99121874 A 19991104**

Priority  
KR 19980055593 A 19981217

Abstract (en)  
A multilayer type chip inductor includes a pair of outermost sheets each of which has a terminal pattern and a first via hole for an electrical connection with neighboring patterns and a plurality of intermediate sheets each of which has a conductor pattern, a second via hole for an electrical connection with neighboring patterns, and a first through hole for reducing a dielectric constant of the inductor. The intermediate sheets are stacked between the outermost sheets in such a way that the conductor patterns thereof are electrically connected with each other and simultaneously are electrically connected with the terminal patterns of the outermost sheets through the first and the second via holes. <IMAGE>

IPC 1-7  
**H01F 17/00**

IPC 8 full level  
**H01F 17/00** (2006.01); **H01F 27/34** (2006.01)

CPC (source: EP KR)  
**H01F 17/00** (2013.01 - KR); **H01F 17/0013** (2013.01 - EP); **H01F 27/34** (2013.01 - EP)

Citation (search report)

- [A] DE 19522043 A1 19961219 - BOSCH GMBH ROBERT [DE]
- [A] PATENT ABSTRACTS OF JAPAN vol. 1996, no. 10 31 October 1996 (1996-10-31)

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Designated contracting state (EPC)  
DE FR GB

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