Title (en)

CMOS DELAY CIRCUIT USING SUBSTRATE BIASSING

Title (de)

CMOS VERZÖGERUNGSSCHALTUNG UNTER VERWENDUNG VON SUBSTRATVORSPANNUNG

Title (fr)

CIRCUIT CMOS A RETARD UTILISANT LA POLARISATION PAR SUBSTRAT

Publication

EP 1016212 A1 20000705 (EN)

Application

EP 99931253 A 19990702

Priority

- EP 99931253 A 19990702
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Abstract (en)

[origin: WO0004638A1] A delay element (DL), for delaying a signal which propagates through the delay element (DL) by a delay, comprises a field effect transistor (T>1<) having a source, a drain, a gate, and a back-gate (BG). The back-gate (BG) is arranged to receive a control voltage (V>cntrl<). The control voltage (V>cntrl<) controls a current through the field effect transistor (T>1<). As a consequence, the delay is also controlled by the control voltage (V>cntrl<).

IPC 1-7

H03K 5/13

IPC 8 full level

H03K 3/354 (2006.01); **H03K 5/13** (2006.01); **H03L 7/099** (2006.01)

CPC (source: EP KR)

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Citation (search report)

See references of WO 0004638A1

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