

Title (en)

METHOD AND APPARATUS FOR HIGH-PERFORMANCE INTEGRATED CIRCUIT INTERCONNECT FABRICATION

Title (de)

METHODE UND APPARAT ZUR HOCHLEISTUNGS-IC-VERDRAHTUNGS-HERSTELLUNG

Title (fr)

PROCEDE ET DISPOSITIF POUR LA REALISATION D'INTERCONNEXIONS SUR CIRCUIT INTEGRE HAUTE PERFORMANCE

Publication

**EP 1018149 A1 20000712 (EN)**

Application

**EP 98947076 A 19980917**

Priority

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Abstract (en)

[origin: WO9914800A1] A method and apparatus for multi-level interconnection fabrication on an integrated circuit are disclosed. A liner/barrier layer (172) and a conductive layer (174) are deposited to fill the trenches and holes in an insulating layer. A globally planarized disposable layer (176) is then formed on the conductive layer (174). The layers are removed at substantially similar rates of material removal, and the removal is stopped when both layers have been removed except for material from the conductive layer filling the trenches and holes. In one implementation, the conductive layer (174) is a copper layer and the globally planarized disposable layer (176) is a tin or tin alloy layer and its formation includes deposition, melting, and resolidification. Further, the removal can be accomplished by an ion-beam etch which is stopped based on in-situ real-time measurement of the wafer surface reflectance. The method employs a cluster tool apparatus.

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IPC 8 full level

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CPC (source: EP KR)

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