Title (en)

A WAY PREDICTION UNIT AND A METHOD FOR OPERATING THE SAME

Title (de)

VORHERSAGEEINHEIT UND VERFAHREN ZUR ANWENDUNG

Title (fr)

UNITE DE PREDICTION DE BLOCS DE MEMOIRE ET SON PROCEDE DE FONCTIONNEMENT

Publication

EP 1019831 A1 20000719 (EN)

Application

EP 96925321 A 19960716

Priority

US 9611755 W 19960716

Abstract (en)

[origin: WO9802817A1] A way prediction unit for a superscalar microprocessor is provided which predicts the next fetch address as well as the way of the instruction cache that the current fetch address hits in while the instructions associated with the current fetch are being read from the instruction cache. The way prediction unit is intended for high frequency microprocessors in which associative caches tend to be clock cycle limiting, causing the instruction fetch mechanism to require more than one clock cycle between fetch requests. Therefore, an instruction fetch can be made every clock cycle using the predicted fetch address until an incorrect next fetch address or an incorrect way is predicted. The instructions from the predicted way are provided to the instruction processing pipelines of the superscalar microprocessor each clock cycle.

IPC 1-7

G06F 12/08

IPC 8 full level

G06F 9/38 (2006.01); **G06F 12/08** (2006.01); **G06F 12/0864** (2016.01)

CPC (source: EP)

G06F 9/3806 (2013.01); **G06F 12/0864** (2013.01); G06F 2212/6082 (2013.01)

Citation (search report)

See references of WO 9802817A1

Designated contracting state (EPC)

DE ES FR GB NL

DOCDB simple family (publication)

WO 9802817 A1 19980122; EP 1019831 A1 20000719

DOCDB simple family (application)

US 9611755 W 19960716; EP 96925321 A 19960716