

Title (en)

SYSTEM FOR LOGIC EXTRACTION FROM A LAYOUT DATABASE

Title (de)

SYSTEM ZUR LOGISCHEN EXTRAKTION AUS EINER DATENBANK-ANORDNUNG

Title (fr)

SYSTEME POUR L'EXTRACTION DE STRUCTURE LOGIQUE D'UNE BASE DE DONNEES D'IMPLANTATION

Publication

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Application

**EP 97912778 A 19971014**

Priority

US 9718844 W 19971014

Abstract (en)

[origin: WO9919818A1] A system and process for logic extraction (15) from the layout of logic blocks (14) is described. Logic design information (15) is extracted from a transistor level net list which is stored in a memory (14). The transistor level net list in turn is generated from a layout polygon database using techniques in the art. The logic extraction process (15) comprises processing the transistor level net list in the memory to define groups of transistors according to whether there is a connection or not to a supply voltage, to a reference voltage, and according to the transistor type (201). The groups of transistors are analyzed according to their interconnections, and their membership in the groups (202). Finally, logic units are identified in response to the step of analyzing groups of transistors (203).

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