

Title (en)  
VERTICAL MOS TRANSISTOR AND METHOD FOR THE PRODUCTION THEREOF

Title (de)  
VERTIKALER MOS-TRANSISTOR UND VERFAHREN ZU DESSEN HERSTELLUNG

Title (fr)  
TRANSISTOR MOS VERTICAL ET SON PROCEDE DE PRODUCTION

Publication  
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Application  
**EP 98955366 A 19981005**

Priority  
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• DE 19746900 A 19971023

Abstract (en)  
[origin: DE19746900A1] A first part (S/D1a) of a first source/drain area (S/D1) is arranged on at least one edge of a semiconductor structure (St) and at least one edge area of a surface (OH) of a semiconductor (St) bordering thereon. The dimension of the first part (S/D1a) of the first source/drain area (S/D1) perpendicular to the edge is smaller than an analogous dimension of the semiconductor structure (St) and smaller than the minimum structural dimension which can be produced according to current technology. In order to produce the inventive transistor, the mask used to make the semiconductor structure can be reduced in size to enable implantation of the first part (S/D1a) of the first source/drain area. In order to facilitate production of the first source/drain area (SD1) contact (K1), a second part (S/D1b) of the first source /drain area (S/D1) can be arranged inside an inner area of the surface (OH) of the semiconductor structure (St). The dimension of the second part (S/D1b) of the first source/drain area (S/D1) perpendicular to the surface (OH) of the semiconductor structure (St) is smaller than the analogous dimension of the first part (S/D1a) of the first source/drain area (S/D1).

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