

Title (en)

METHOD OF EMULATING A SHIFT REGISTER USING A RAM

Title (de)

VERFAHREN ZUM EMULIEREN EINES SCHIEBEREGISTERS UNTER BENUTZUNG EINES RAM'S

Title (fr)

PROCEDE D'EMULATION D'UN REGISTRE A DECALAGE AU MOYEN D'UNE MEMOIRE RAM

Publication

EP 1027649 A1 20000816 (EN)

Application

EP 98947185 A 19980918

Priority

- US 9819708 W 19980918
- US 94746797 A 19971009

Abstract (en)

[origin: WO9919798A1] A method using a RAM (10) and a short shift register (20) to emulate a long shift register to store a stream of incoming bits. A pointer points to one of the RAM registers. To store an incoming bit, the contents of the RAM register pointed to by the pointer are written to the shift register (20) and shifted by one bit, the incoming bit is stored in the location in the shift register (20) freed up by the shift operation, the updated contents of the shift register (20) are written back to the RAM register pointed to by the pointer, and the pointer is incremented.

IPC 1-7

G06F 9/445; G06F 5/06

IPC 8 full level

G06F 5/08 (2006.01); **G06F 5/10** (2006.01); **G11C 19/00** (2006.01)

CPC (source: EP KR)

G06F 5/08 (2013.01 - EP KR); **G06F 5/10** (2013.01 - EP KR); **G06F 2205/104** (2013.01 - EP)

Designated contracting state (EPC)

DE FR GB IT

DOCDB simple family (publication)

WO 9919798 A1 19990422; AU 9402098 A 19990503; CN 1119745 C 20030827; CN 1281559 A 20010124; EP 1027649 A1 20000816; EP 1027649 A4 20040804; JP 2001520429 A 20011030; KR 20010024466 A 20010326

DOCDB simple family (application)

US 9819708 W 19980918; AU 9402098 A 19980918; CN 98810664 A 19980918; EP 98947185 A 19980918; JP 2000516283 A 19980918; KR 20007003819 A 20000408