Title (en)
HIGH-PERFORMANCE ARCHITECTURE FOR DISK ARRAY CONTROLLER

Title (de)
HOCHLEISTUNGSARCHITEKTUR FÜR SPEICHERPLATTENANORDNUNGSSTEUERUNGSVORRICHTUNG

Title (fr)
ARCHITECTURE HAUTE PERFORMANCE POUR CONTROLEUR DE GRAPPE DE DISQUES

Publication
EP 1031091 A1 20000830 (EN)

Application
EP 98950997 A 19981008

Priority
- US 9821203 W 19981008
- US 6584897 P 19971114
- US 3424798 A 19980304
- US 3424898 A 19980304
- US 3481298 A 19980304

Abstract (en)
[origin: WO9926150A1] A high-performance RAID system for a PC comprises a controller card (70) which controls an array of ATA disk drives (72). The controller card (70) includes an array of automated disk drive controllers (84), each of which controls one respective disk drive (72). The disk drive controllers (84) are connected to a microcontroller (82) by a control bus (86) and are connected to an automated coprocessor (80) by a packet-switched bus (90). The coprocessor (80) accesses system memory (40) and a local buffer (94). In operation, the disk drive controllers (84) respond to controller commands from the microcontroller (82) by accessing their respective disk drives (72), and by sending packets to the coprocessor (80) over the packet-switched bus (90). The packets carry I/O data (in both directions, with the coprocessor filling-in packet payloads on I/O writes), and carry transfer commands and target addresses that are used by the coprocessor (80) to access the buffer (94) and system memory (40). The packets also carry special completion values (generated by the microcontroller) and I/O request identifiers that are processed by a logic circuit (144) of the coprocessor (80) to detect the completion of processing of each I/O request. The coprocessor (80) grants the packet-switched bus (90) to the desk drive controllers (84) using a round robin arbitration protocol which guarantees a minimum I/O bandwidth to each disk drive (72). This minimum I/O bandwidth is preferably greater than the sustained transfer rate of each disk drive (72), so that all drives of the array can operate at the sustained transfer rate without the formation of a bottleneck.

IPC 1-7
G06F 13/14; G06F 13/00; G06F 13/10; G06F 13/12

IPC 8 full level
G06F 13/14 (2006.01); **G06F 3/06** (2006.01); **G06F 13/10** (2006.01); **G06F 13/12** (2006.01)

CPC (source: EP)
G06F 3/0613 (2013.01); **G06F 3/0658** (2013.01); **G06F 3/0689** (2013.01); **G06F 13/124** (2013.01)

Designated contracting state (EPC)
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

DOCDB simple family (publication)
WO 9926150 A1 19990527; AU 9689898 A 19990607; EP 1031091 A1 20000830; EP 1031091 A4 20021106; JP 2001523860 A 20011127

DOCDB simple family (application)
US 9821203 W 19981008; AU 9689898 A 19981008; EP 98950997 A 19981008; JP 2000521447 A 19981008