

Title (en)

Process of manufacturing electronic virtual ground memory devices

Title (de)

Herstellungsverfahren für elektronische Speicheranordnungen mit Zellenmatrix mit virtueller Erdung

Title (fr)

Procédé de fabrication de dispositifs électroniques de mémoire avec matrice de cellules à masse virtuelle

Publication

EP 1032035 A1 20000830 (EN)

Application

EP 99830100 A 19990226

Priority

EP 99830100 A 19990226

Abstract (en)

A process for manufacturing electronic semiconductor integrated electronic memory devices having virtual ground and comprising at least a matrix of floating gate memory cells (1), the matrix being formed on a semiconductor substrate (2) with a plurality of continuous bit lines (10) extending across the substrate (2) as discrete parallel strips, comprising at least the following steps: forming an oxide layer (3) over the matrix region; depositing the semiconductor throughout with a stack structure which comprises a first conductor layer (4), first dielectric layer (5), and second conductor layer (6); forming a second dielectric layer (7); defining floating gate regions (13) by photolithography using a mask of "POLY1 along a first predetermined direction", and associated etching, to define, in said stack structure, a plurality of parallel openings (9); implanting said parallel openings (9) to confer a predetermined conductivity on the bit line (10) regions; filling the parallel openings (12) with a photo-sensitive material (11) to protect the matrix bit lines (10). <IMAGE>

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Citation (search report)

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- [Y] PATENT ABSTRACTS OF JAPAN vol. 004, no. 126 (E - 024) 5 September 1980 (1980-09-05)
- [A] PATENT ABSTRACTS OF JAPAN vol. 009, no. 193 (E - 334) 9 August 1985 (1985-08-09)

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