

Title (en)
MOS-gated device having a buried gate and process for forming same

Title (de)
MOS-Anordnung mit einer vergrabenen Gate und Verfahren zur Herstellung

Title (fr)
Dispositif MOS à grille enterrée et procédé pour sa fabrication

Publication
EP 1033759 B1 20121003 (EN)

Application
EP 00102398 A 20000203

Priority
US 26041199 A 19990301

Abstract (en)
[origin: EP1033759A2] An improved trench MOS-gated device comprises a monocrystalline semiconductor substrate on which is disposed a doped upper layer. The upper layer includes at an upper surface a plurality of heavily doped body regions having a first polarity and overlying a drain region. The upper layer further includes at its upper surface a plurality of heavily doped source regions having a second polarity opposite that of the body regions. A gate trench extends from the upper surface of the upper layer to the drain region and separates one source region from another. The trench has a floor and sidewalls comprising a layer of dielectric material and contains a conductive gate material filled to a selected level and an isolation layer of dielectric material that overlies the gate material and substantially fills the trench. The upper surface of the overlying layer of dielectric material in the trench is thus substantially coplanar with the upper surface of the upper layer. A process for forming an improved MOS-gate device provides a device whose gate trench is filled to a selected level with a conductive gate material, over which is formed an isolation dielectric layer whose upper surface is substantially coplanar with the upper surface of the upper layer of the device. <IMAGE>

IPC 8 full level
H01L 29/78 (2006.01); **H01L 21/331** (2006.01); **H01L 21/332** (2006.01); **H01L 21/336** (2006.01); **H01L 29/06** (2006.01); **H01L 29/423** (2006.01); **H01L 29/739** (2006.01); **H01L 29/74** (2006.01); **H01L 31/062** (2006.01)

CPC (source: EP KR US)
H01L 29/0696 (2013.01 - EP US); **H01L 29/4236** (2013.01 - EP KR US); **H01L 29/66348** (2013.01 - EP US); **H01L 29/66734** (2013.01 - EP KR US); **H01L 29/7397** (2013.01 - EP US); **H01L 29/7813** (2013.01 - EP KR US)

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EP1708276A4; EP2491581A4; EP1244150A3; US7388254B2; US10229988B2; US9761696B2; US9947770B2; US9887259B2; US10283587B2; US9882044B2; US10084037B2; US10340377B2; US10234486B2; US10444262B2; US10527654B2; EP1599907A4

Designated contracting state (EPC)
DE DK FR GB IT

DOCDB simple family (publication)
EP 1033759 A2 20000906; **EP 1033759 A3 20001122**; **EP 1033759 B1 20121003**; EP 2280418 A1 20110202; JP 2000252468 A 20000914; JP 5118270 B2 20130116; KR 100714198 B1 20070502; KR 20000076758 A 20001226; TW 452890 B 20010901; US 2002056871 A1 20020516; US 2005224868 A1 20051013; US 2008116510 A1 20080522; US 2008121989 A1 20080529; US 6351009 B1 20020226; US 6916712 B2 20050712; US 7388254 B2 20080617

DOCDB simple family (application)
EP 00102398 A 20000203; EP 10180114 A 20000203; JP 2000044636 A 20000222; KR 20000010358 A 20000302; TW 89102283 A 20000211; US 26041199 A 19990301; US 3931901 A 20011109; US 9173305 A 20050328; US 93037107 A 20071031; US 93038007 A 20071031