

Title (en)

METHOD FOR THINNING SEMICONDUCTOR WAFERS WITH CIRCUITS AND WAFERS MADE BY THE SAME

Title (de)

VERFAHREN ZUR VERMINDERUNG DER DICKE VON SCHALTUNGEN ENTHALTENDEN HALBLEITERSCHEIBEN UND DADURCH HERGESTELLTE SCHEIBEN

Title (fr)

PROCEDE D'AMINCISSEMENT DE PLAQUETTES EN SEMI-CONDUCTEUR A CIRCUITS ET PLAQUETTES AINSI PRODUITES

Publication

EP 1038315 A4 20010711 (EN)

Application

EP 98957755 A 19981110

Priority

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Abstract (en)

[origin: WO9925019A1] Thinned and/or flexible integrated circuit chips (34) are fabricated by defining a plurality of grooves (30) into the front surface of a semiconductor wafer (22). The grooves (30) isolate each integrated circuit into a separate die. The prescribed grooves extend only partially into the front surface in which the circuits are formed, typically 50 microns or less (32). A polyimide planarizing and stress relieving layer is disposed on the front surface before the grooves are grooved. A low viscosity low stress adhesive is disposed on the grooved polyimide coated surface. The wafer is then bonded to the scored surface of an optically flat glass substrate under pressure and at a curing temperature. The assembly is then mounted into a grinder which removes the backside portion of the wafer until the grooves are exposed. Grinding is achieved by advancing at a decreasing grind rate followed by periods of dwell. The grooves in the semiconductor wafer tend to inhibit crack formation. The assembly is then placed backside down on a pin block in a solvent bath. The solvent dissolves the adhesive layer leaving the separated dies of the pin block for mounting on a flexible film. The dies are coupled to metalizations on the flexible film by means of a conductive epoxy and sealed using a flexible coating.

IPC 1-7

H01L 21/78; **H01L 25/065**; **H01L 21/68**; **H01L 21/60**; **H01L 23/498**

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CPC (source: EP)

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Citation (search report)

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- See references of WO 9925019A1

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