

Title (en)

Semiconductor integrated circuit and semiconductor memory device including overdriving sense amplifier

Title (de)

Integrierte Halbleiterschaltung und Halbleiterspeicheranordnung mit Leseverstärkerübersteuerung

Title (fr)

Circuit intégré à semi-conducteurs et dispositif de mémoire à semi-conducteurs avec surcharge de l' amplificateur de lecture

Publication

EP 1039471 A3 20001108 (EN)

Application

EP 00301046 A 20000210

Priority

- JP 8451099 A 19990326
- JP 8471599 A 19990326

Abstract (en)

[origin: EP1039471A2] A transistor (11) of a driver (5) in a semiconductor integrated circuit has its gate connected to a controlling circuit (41), and has its drain connected to a sense amplifier (AMP). The controlling circuit (41) supplies the gate of the transistor (11) with a gate-to-source voltage exceeding or below other power supply voltages. The drain-to-source resistance of the transistor (11) in the on state becomes sufficiently lower as compared with that in the case of supplying the power supply voltages between the gate and source of the transistor (11). Accordingly, the amplifying speed of the sense amplifier (AMP) is heightened without altering the sense amplifier (AMP) and the driver (5). Besides, the amplifying speed of the sense amplifier (AMP) is heightened without raising the power supply voltage which supplies the carriers to the driver (5). <IMAGE>

IPC 1-7

G11C 7/00; G11C 5/14

IPC 8 full level

G11C 7/06 (2006.01); **G11C 7/22** (2006.01)

CPC (source: EP KR US)

G11C 5/14 (2013.01 - EP US); **G11C 5/147** (2013.01 - KR); **G11C 7/065** (2013.01 - EP US); **G11C 7/08** (2013.01 - EP KR US); **G11C 11/4074** (2013.01 - EP KR US); **G11C 11/4091** (2013.01 - EP KR US); **G11C 29/021** (2013.01 - EP US); **G11C 29/028** (2013.01 - EP US); **G11C 5/025** (2013.01 - EP US); **G11C 7/065** (2013.01 - KR); **G11C 29/02** (2013.01 - EP US); **G11C 2207/065** (2013.01 - EP KR US)

Citation (search report)

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