

Title (en)
AN ATM CELL PROCESSOR

Title (de)
EIN ATM-ZELLENPROZESSOR

Title (fr)
PROCESSEUR DE CELLULES A MODE DE TRANSFERT ASYNCHRONE

Publication
EP 1040707 A2 20001004 (EN)

Application
EP 98961336 A 19981215

Priority

- IE 9800106 W 19981215
- IE 970888 A 19971215
- IE S980712 A 19980831

Abstract (en)
[origin: WO9931928A2] An ATM cell processor (10) has a backplane interface (11), a line interface (15), and various processing functions between the interfaces. Cells directed to the line interface (15) are controlled by a queueing function (12) which uses external cell memory via a controller (13) and external control memory via a controller (14). Cells from the backplane are identified and routed by a mapping function (16).

IPC 1-7
H04Q 11/04; **H04L 12/56**

IPC 8 full level
H04L 12/54 (2013.01); **H04L 12/56** (2006.01); **H04L 12/935** (2013.01); **H04L 12/937** (2013.01); **H04Q 11/04** (2006.01); **H04L 12/70** (2013.01)

CPC (source: EP)
H04L 12/5601 (2013.01); **H04L 49/255** (2013.01); **H04L 49/3081** (2013.01); **H04Q 11/0478** (2013.01); **H04L 2012/5658** (2013.01); **H04L 2012/5681** (2013.01)

Citation (search report)
See references of WO 9931928A2

Designated contracting state (EPC)
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

DOCDB simple family (publication)
WO 9931928 A2 19990624; **WO 9931928 A3 19991028**; AU 1680499 A 19990705; CA 2315052 A1 19990624; EP 1040707 A2 20001004; IE S80918 B2 19990630; IE S980712 A2 19990630; JP 2002509412 A 20020326

DOCDB simple family (application)
IE 9800106 W 19981215; AU 1680499 A 19981215; CA 2315052 A 19981215; EP 98961336 A 19981215; IE S980712 A 19980831; JP 2000539674 A 19981215