

Title (en)

Method of fabrication of a high voltage MOS transistor

Title (de)

Verfahren zur Herstellung eines Hochspannungs-MOS-Feldeffekttransistors

Title (fr)

Méthode de fabrication d'un transistor à effet de champ du type MOS pour haute tension

Publication

EP 1043778 A1 20001011 (EN)

Application

EP 99830194 A 19990406

Priority

EP 99830194 A 19990406

Abstract (en)

Method of fabrication of a no-field transistor with no extra process costs, providing for defining an active area for the transistor surrounded by a thick field oxide layer (3), insulatively placing a polysilicon gate electrode (40) across the active area to define source/drain regions (50) of the no-field transistor, providing an implant protection mask (60) over a boundary (2) between at least one of the source/drain regions and the field oxide layer, selectively implanting in said source/drain regions a relatively heavy dose of dopants to form relatively heavily doped source/drain regions and to simultaneously dope the polysilicon gate electrode, characterized in that said polysilicon gate electrode is formed with lateral wings (41) extending towards said at least one source/drain region, and in that said implant protection mask (60) extends over said lateral wings but not over the polysilicon gate (40). <IMAGE>

IPC 1-7

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IPC 8 full level

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CPC (source: EP US)

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Citation (search report)

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- [A] US 5396096 A 19950307 - AKAMATSU SUSUMU [JP], et al
- [XA] PATENT ABSTRACTS OF JAPAN vol. 012, no. 099 (E - 594) 31 March 1988 (1988-03-31)
- [A] PATENT ABSTRACTS OF JAPAN vol. 013, no. 144 (E - 740) 10 April 1989 (1989-04-10)
- [A] OISHI T ET AL: "NOTICEABLE ENHANCEMENT OF EDGE EFFECT IN SHORT CHANNEL CHARACTERISTICS OF TRENCH-ISOLATED MOSFETS", INTERNATIONAL CONFERENCE ON SOLID STATE DEVICES AND MATERIALS,JA,JAPAN SOCIETY OF APPLIED PHYSICS. TOKYO, September 1998 (1998-09-01), pages 86 - 87, XP000823084
- [A] PATENT ABSTRACTS OF JAPAN vol. 017, no. 035 (E - 1310) 22 January 1993 (1993-01-22)

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