

Title (en)
CMOS inverter and standard cell using the same

Title (de)
CMOS Inverter und diesen verwendende Standardzelle

Title (fr)
Inverseur CMOS et cellule standard utilisant celui-ci

Publication
EP 1049166 A3 20041020 (EN)

Application
EP 99112822 A 19990702

Priority
JP 11929099 A 19990427

Abstract (en)
[origin: EP1049166A2] **Problem** To prevent a void from being formed in a CMOS inverter due to electromigration. **Solution** Means for Solving the Problem A power line 11 is connected to the source of a p-channel MOS transistor Tr1 via a first contact 12. A ground line 13 is connected to the source of an n-channel MOS transistor Tr2 via a second contact 14. One terminal of a first output signal line 15 is connected to the drain of the p-channel MOS transistor Tr1 via a third contact 16, while the other terminal thereof is connected to the drain of the n-channel MOS transistor Tr2 via a fourth contact 17. One terminal of a second output signal line 18 is connected to the fourth contact 17, while the other terminal thereof extends toward the output terminal of the inverter. A first path of an input signal line 19 is connected to the gate electrode 20 of the p-channel MOS transistor Tr1 via a fifth contact 21, while a second path thereof is connected to the gate electrode 20 of the n-channel MOS transistor Tr2 via a sixth contact 22. **IMAGE**

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H01L 27/092; **H01L 27/02**

IPC 8 full level
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CPC (source: EP KR US)
H01L 27/08 (2013.01 - KR); **H01L 27/092** (2013.01 - EP US); **H01L 2924/0002** (2013.01 - EP US)

Citation (search report)
• [XY] US 5532509 A 19960702 - D ADDEO MICHAEL L [US]
• [Y] EP 0574097 A2 19931215 - TOSHIBA KK [JP]
• [X] US 5528061 A 19960618 - IWASAKI TADASHI [JP]
• [X] EP 0324459 A2 19890719 - FUJITSU LTD [JP]
• [Y] PATENT ABSTRACTS OF JAPAN vol. 017, no. 257 (E - 1368) 20 May 1993 (1993-05-20)
• [A] PATENT ABSTRACTS OF JAPAN vol. 1998, no. 10 31 August 1998 (1998-08-31) & US 2001015464 A1 20010823 - TAMAKI TOKUHIKO [JP]

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