Title (en)

MEMORY CELL ARRANGEMENT AND METHOD FOR PRODUCING THE SAME

Title (de)

SPEICHERZELLENANORDNUNG UND ENTSPRECHENDES HERSTELLUNGSVERFAHREN

Title (fr)

ENSEMBLE DE CELLULES DE MEMOIRE ET SON PROCEDE DE FABRICATION

Publication

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Application

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Abstract (en)

[origin: DE19807920A1] The invention relates to a memory cell arrangement, comprising a number of memory cells (S) arranged in a semiconductor substrate (10) with bit line trenches (1a-1d) running parallel in a longitudinal direction in the main surface of the semiconductor substrate (10). Each bit line trench (1a-1d) is provided with a first conductive area (15a-15d) in the bottom and a second conductive area (20a-20e) of the same conduction type in the top, with a channel area being provided in between in the walls of each trench. Word lines (2a-2c) run in a crosswise direction along the main surface of the semiconductor substrate (10) through certain bit line trenches (1a, 1c, 1d) for controlling the transistors provided there. An additional dopant is introduced into the trench walls of the bit line trenches (1a-1d) situated between the word lines (2a-2c) in order to increase the corresponding transistor cutoff voltage for preventing leakage currents.

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