

Title (en)
METHOD OF WIRE BONDING, SEMICONDUCTOR DEVICE, CIRCUIT BOARD, ELECTRONIC DEVICE AND WIRE BONDER

Title (de)
DRAHTBAND-METHODE, HALBLEITER, LEITERPLATTE, ELEKTRONIKELEMENT UND DRAHTBANDER

Title (fr)
TECHNIQUE DE SOUDAGE DE FILS, DISPOSITIF SEMI-CONDUCTEUR, CARTE DE CIRCUIT IMPRIME, DISPOSITIF ELECTRONIQUE ET POSTE DE SOUDURE

Publication
EP 1069608 A4 20040811 (EN)

Application
EP 00900809 A 20000119

Priority

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- JP 1382599 A 19990122

Abstract (en)
[origin: EP1069608A1] A wire bonding method comprising: disposing a plurality of leads (20) aligned in an imaginary plane (P) around the periphery of a semiconductor chip (10) having a plurality of electrodes (12) aligned on an imaginary straight line (L1); bonding wires (30) to the electrodes (12); bending the wires (30) toward the leads (20) as viewed from a direction perpendicular to the imaginary plane (P); and bonding the wires (30) to the leads (20). <IMAGE>

IPC 1-7
H01L 21/60; **H01L 21/00**; **H01L 23/495**

IPC 8 full level
H01L 21/60 (2006.01); **H01L 21/607** (2006.01); **H01L 23/495** (2006.01)

CPC (source: EP KR US)
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Citation (search report)

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DE FR GB

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EP 1069608 A1 20010117; **EP 1069608 A4 20040811**; **EP 1069608 B1 20070314**; DE 60033888 D1 20070426; JP 2000216188 A 20000804; KR 100388728 B1 20030625; KR 20010092255 A 20011024; TW 480633 B 20020321; US 6437453 B1 20020820; WO 0044040 A1 20000727

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