

Title (en)

GLOBAL SIGNAL DISTRIBUTION ARCHITECTURE IN A FIELD PROGRAMMABLE GATE ARRAY

Title (de)

ARCHITEKTUR ZUR VERTEILUNG VON GLOBALEN SIGNALEN IN EINEM NUTZERPROGRAMMIERBAREN GATTERFELD

Title (fr)

ARCHITECTURE DE DISTRIBUTION D'UN SIGNAL GLOBAL DANS UN RESEAU DE PORTES PROGRAMMABLE PAR L'UTILISATEUR

Publication

EP 1078462 A4 20010613 (EN)

Application

EP 00913563 A 20000222

Priority

- US 0004477 W 20000222
- US 25506099 A 19990222

Abstract (en)

[origin: WO0049718A1] A global signal distribution architecture for an FPGA architecture that has a plurality of multiplexers (80) with inputs and an output. The outputs of the plurality of multiplexers (80) are coupled to global I/O lines (16) that are coupled to a global signal distribution bus (18) spanning a highest level in the FPGA architecture. A plurality of switch matrices (106) are coupled to global signal distribution bus (18) and to a plurality of utility conductors (108) that are coupled to at least one multiplexer associated with a lowest level in the FPGA architecture.

IPC 1-7

H03K 19/177; H01L 25/00

IPC 8 full level

H03K 19/177 (2006.01)

CPC (source: EP)

H03K 19/17736 (2013.01)

Citation (search report)

- [X] US 5371422 A 19941206 - PATEL RAKESH H [US], et al
- [X] DAVE BURSKEY: "Variable-Grain Architecture Pumps UP FPGA Performance", ELECTRONIC DESIGN, vol. 46, no. 4, 23 February 1998 (1998-02-23), pages 102,104,106, XP002165019
- See references of WO 0049718A1

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