

Title (en)
PROCESS AND MANUFACTURING TOOL ARCHITECTURE FOR USE IN THE MANUFACTURE OF ONE OR MORE METALLIZATION LEVELS ON A WORKPIECE

Title (de)
VERFAHREN UND ANORDNUNG EINER HERSTELLUNGSVORRICHTUNG ZUR VERWENDUNG IN DER HERSTELLUNG EINES ODER MEHRERER METALLISIERUNGSNIVEAUS AUF EINEM WERKSTÜCK

Title (fr)
OUTIL SERVANT A FABRIQUER UN OU PLUSIEURS NIVEAUX DE METALLISATION SUR UN COMPOSANT A SEMICONDUCTEUR ET PROCEDE CORRESPONDANT

Publication
EP 1086485 A2 20010328 (EN)

Application
EP 99922934 A 19990512

Priority
• US 9910331 W 19990512
• US 7656598 A 19980512
• US 7669598 A 19980512
• US 12823898 A 19980803

Abstract (en)
[origin: WO9959190A2] A semiconductor manufacturing tool configuration and corresponding process for applying one or more levels of interconnect metallization to a generally planar dielectric surface of a semiconductor workpiece with a minimal number of workpiece transfer operations between the tool sets is disclosed.

IPC 1-7
H01L 21/00

IPC 8 full level
C12N 15/31 (2006.01); **H01L 21/302** (2006.01); **H01L 21/304** (2006.01); **H01L 21/306** (2006.01); **H01L 21/3065** (2006.01); **H01L 21/3213** (2006.01); **H01L 21/768** (2006.01); **H01L 37/00** (2006.01)

CPC (source: EP)
H01L 21/32134 (2013.01); **H01L 21/76852** (2013.01); **H01L 21/76885** (2013.01); **H01L 21/76825** (2013.01); **H01L 21/76826** (2013.01); **H01L 21/76888** (2013.01)

Citation (search report)
See references of WO 9959190A2

Designated contracting state (EPC)
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

DOCDB simple family (publication)
WO 9959190 A2 19991118; **WO 9959190 A3 20000406**; EP 1086485 A2 20010328; JP 2002515645 A 20020528; TW 494443 B 20020711

DOCDB simple family (application)
US 9910331 W 19990512; EP 99922934 A 19990512; JP 2000548908 A 19990512; TW 88107682 A 19990512