

Title (en)  
Linear regulator with output voltage selection

Title (de)  
Linearer Regler mit Ausgangsspannungsauswahl

Title (fr)  
Régulateur linéaire à sélection de la tension de sortie

Publication  
**EP 1089154 A1 20010404 (FR)**

Application  
**EP 00410119 A 20000928**

Priority  
FR 9912524 A 19991001

Abstract (en)  
The linear regulator (20), as of known type, comprises a MOS power transistor (2) controlled by a differential amplifier (5) with the inverted input (7) receiving a reference voltage (Vref) and the non-inverted input (8) receiving, by the intermediary of a circuit (10') with resistances switching, a selection of output voltage (Vout), for the purpose of soft switching of resistances. The resistances (R1,R2,R3) of a divider bridge are being switched by means of two MOS control transistors (12,14) with the gates receiving the inverted voltage slope signals (CTRL1',CTRL2') generated by two control circuits (21,22), preferentially identical and of spherical structure. The length of voltage slopes (CTRL1',CTRL2') is chosen so as to maintain, at the input (8) of differential amplifier (5), a voltage level corresponding substantially to the level of reference voltage (Vref), which is the same during the switching phase, and to avoid unbalancing the differential amplifier. The inverted voltage slope signals (CTRL1', CTRL2') have the signs fixed by the switching, and are obtained from the standard control signals by use of control circuits (21,22). Each control circuit (21,22) comprises two transistors with opposite conductivity channels connected in series between supply terminals, where the midpoint of connection by aid of a capacitor delivers the voltage slope signal. The MOS power transistor (2) is of p-type conductivity channel, and the MOS control transistors are with the same type conductivity channels.

Abstract (fr)  
L'invention concerne un procédé de commande et un régulateur linéaire (20) du type comprenant un transistor MOS de puissance (2), commandé par un amplificateur différentiel (5) dont une première borne d'entrée (7) reçoit une tension de référence (Vref) et dont une deuxième borne d'entrée (8) reçoit, par 1 'intermédiaire d'un circuit (10') de résistances commutables, la tension de sortie (Vout) du régulateur, une commutation douce desdites résistances étant organisée. <IMAGE>

IPC 1-7  
**G05F 1/563**

IPC 8 full level  
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CPC (source: EP US)  
**G05F 1/563** (2013.01 - EP US); **G05F 1/565** (2013.01 - EP US); **G05F 1/575** (2013.01 - EP US)

Citation (search report)  
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