Title (en)

Encryption circuit architecture implementing simultaneously different encryption algorithms whithout losing performance

Title (de)

Verschlüsselungsschaltungsarchitektur zur gleichzeitigen Ausführung mehrerer Verschlüsselungsalgorithmen ohne Leistungseinbusse

Title (fr)

Architecture d'un circuit de chiffrement mettant en oeuvre différents types d'algorithmes de chiffrement simultanément sans perte de performance

Publication

EP 1100225 B1 20050615 (FR)

Application

EP 00403063 A 20001106

Priority

FR 9914067 A 19991109

Abstract (en)

[origin: EP1100225A1] Circuit (1) comprises an I/O module (2) for data exchange between a host system (HS) and the circuit via a dedicated PCI bus, an encryption module (3) for encryption or decryption as well as storing sensitive data and an isolation device (4) between the I/O module and the encryption module preventing the host system from accessing the encryption module during its parallel processing.

IPC 1-7

H04L 9/00; G06F 9/06; H04L 9/08

IPC 8 full level

G06F 12/14 (2006.01); **G06F 13/38** (2006.01); **G06F 21/72** (2013.01); **H04L 9/00** (2006.01); **H04L 9/08** (2006.01); **H04L 9/10** (2006.01); **H04L 9/14** (2006.01)

CPC (source: EP US)

G06F 21/72 (2013.01 - EP US); **H04L 9/14** (2013.01 - EP US)

Cited by

FR3003712A1

Designated contracting state (EPC)

DE FR GB

DOCDB simple family (publication)

EP 1100225 A1 20010516; **EP 1100225 B1 20050615**; DE 60020794 D1 20050721; DE 60020794 T2 20060504; FR 2800952 A1 20010511; FR 2800952 B1 20011207; JP 2001211163 A 20010803; JP 4138225 B2 20080827; US 2007223688 A1 20070927; US 7418598 B1 20080826

DOCDB simple family (application)

EP 00403063 A 20001106; DE 60020794 T 20001106; FR 9914067 A 19991109; JP 2000340881 A 20001108; US 70672800 A 20001107; US 80275907 A 20070524