Title (en)

METHOD AND APPARATUS FOR BUILT-IN SELF TEST OF INTEGRATED CIRCUITS

Title (de)

VERFAHREN UND APPARAT ZUM EINGEBAUTEN SELBSTTESTEN VON INTEGRIERTEN SCHALTUNGEN

Title (fr)

PROCEDE ET APPAREIL POUR AUTOCONTROLE DE CIRCUITS INTEGRES

Publication

EP 1105876 A4 20030917 (EN)

Application

EP 98945762 A 19980821

Priority

US 9817298 W 19980821

Abstract (en)

[origin: WO0011674A1] A BIST function is provided in which both the row address (50) and the column address (40) of a memory (90) to be tested may be selected independently. The present invention provides flexibility in selecting address to be tested, improves transition time between rows, and allows determination of which memory address passes or fails the test.

IPC 1-7

G01R 31/3187; G01R 31/3193

IPC 8 full level

G01R 31/28 (2006.01); **G06F 11/22** (2006.01); **G06F 12/16** (2006.01); **G11C 11/401** (2006.01); **G11C 11/413** (2006.01); **G11C 16/02** (2006.01); **G11C 17/00** (2006.01); **G11C 29/12** (2006.01); **G11C 29/18** (2006.01)

CPC (source: EP KR)

G11C 7/00 (2013.01 - KR); **G11C 29/18** (2013.01 - EP)

Citation (search report)

- [XY] EP 0492624 A1 19920701 - TOSHIBA KK [JP], et al
- [Y] US 5258986 A 19931102 - ZERBE JARED L [US]
- [Y] US 5477494 A 19951219 - MIYAGAWA TADATOSHI [JP], et al
- [A] US 5615159 A 19970325 - ROOHPARVAR FRANKIE F [US]
- [A] US 5588111 A 19961224 - CUTTS JR RICHARD W [US], et al
- [A] US 5659551 A 19970819 - HUOTT WILLIAM VINCENT [US], et al
- [A] US 5661732 A 19970826 - LO TIN-CHEE [US], et al
- See references of WO 0011674A1

Designated contracting state (EPC)

DE FR GB NL

DOCDB simple family (publication)

WO 0011674 A1 20000302; EP 1105876 A1 20010613; EP 1105876 A4 20030917; JP 2002523854 A 20020730; KR 100589532 B1 20060613; KR 20010052985 A 20010625

DOCDB simple family (application)

US 9817298 W 19980821; EP 98945762 A 19980821; JP 2000566851 A 19980821; KR 20007014379 A 20001218