Title (en)
Cache with multiple fill modes

Title (de)
Cachespeicher mit mehreren Füllungsmoden

Title (fr)
Antémémoire avec plusieurs modes de remplissage

Publication
**EP 1111511 B1 20170927 (EN)**

Application
**EP 99403041 A 19991206**

Priority
EP 99403041 A 19991206

Abstract (en)
[origin: EP1111511A1] A cache architecture (16) for use in a processing device includes a RAM set cache for caching a contiguous block of main memory. The RAM set cache can be used in conjunction with other cache types, such as a set associative cache or a direct mapped cache. A register (32) defines a starting address for the contiguous block of main memory. The data array (38) associated with the RAM set may be filled on a line-by-line basis, as lines are requested by the processing core, or on a set-fill basis which fills the data array (38) when the starting address is loaded into the register (32). As addresses are received from the processing core, hit/miss logic (46) the starting address register (32), a global valid bit (34), line valid bits (37) and control bits (24, 26) are used to determine whether the data is present in the RAM set or whether the data must be loaded from main memory . The hit/miss logic (46) also determines whether a line should be loaded into the RAM set data array (38) or in the associated cache. <IMAGE>

IPC 8 full level
**G06F 13/00** (2006.01); **G06F 13/28** (2006.01); **G06F 12/0802** (2016.01); **G06F 12/0862** (2016.01); G06F 12/0864 (2016.01); G06F 12/0895 (2016.01)

CPC (source: EP KR US)
**G06F 12/0802** (2013.01 - EP US); **G06F 12/0862** (2013.01 - EP US); **G06F 13/00** (2013.01 - KR); **G06F 13/28** (2013.01 - US); G06F 12/0864 (2013.01 - EP); G06F 12/0895 (2013.01 - EP); G06F 2212/1016 (2013.01 - EP); G06F 2212/2515 (2013.01 - EP US)

Cited by
US6789172B2; EP1489490A3; CN104778130A; EP2090987A1; GB2454811B; GB2454811A; US7330937B2; US8069308B2; US11409643B2; US8725987B2; US9208096B2; US9311246B2

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