

Title (en)

Instantaneous fault detection circuit method and apparatus

Title (de)

Sofort reagierende Fehlererfassungsschaltung, sowie Verfahren und Gerät hierzu

Title (fr)

Circuit de détection de défaut instantané, procédé et dispositif

Publication

**EP 1111752 A2 20010627 (EN)**

Application

**EP 00311485 A 20001220**

Priority

US 46774499 A 19991220

Abstract (en)

An algorithmic system for an electronic trip unit (30) is provided whereby reliable instantaneous protection is provided. A multi-algorithmic approach uses an algorithm (74) to detect bolted faults based on a direct comparison of the current and a threshold value, and an additional algorithm (90) to detect current overloads based on a comparison (96) of a peak-to-peak current (94) and an additional current threshold. <IMAGE>

IPC 1-7

**H02H 7/30**; **H02H 1/00**

IPC 8 full level

**H02H 1/00** (2006.01); **H02H 7/30** (2006.01); **H02H 1/04** (2006.01)

CPC (source: EP US)

**H02H 1/0092** (2013.01 - EP US); **H02H 7/30** (2013.01 - EP US); **H02H 1/04** (2013.01 - EP US)

Citation (applicant)

US 5237511 A 19930817 - CAIRD KENNETH J [CA], et al

Designated contracting state (EPC)

DE FR

DOCDB simple family (publication)

**EP 1111752 A2 20010627**; **EP 1111752 A3 20050824**; **EP 1111752 B1 20100623**; CN 1306329 A 20010801; CN 1331287 C 20070808; DE 60044575 D1 20100805; US 2003107860 A1 20030612; US 6545849 B1 20030408; US 7016174 B2 20060321

DOCDB simple family (application)

**EP 00311485 A 20001220**; CN 00137071 A 20001220; DE 60044575 T 20001220; US 34806103 A 20030120; US 46774499 A 19991220