Title (en)

BUILT-IN SELF TEST SCHEMES AND TESTING ALGORITHMS FOR RANDOM ACCESS MEMORIES

Title (de)

EINGEBAUTEN SELBSTTESTSSCHEMA UND TESTALGORITHMEN FÜR DIREKTZUGRIFFSPEICHER

Title (fr)

SYSTEMES D'AUTO-CONTROLE INTEGRES ET ALGORITHMES DE CONTROLE POUR MEMOIRES A ACCES ALEATOIRES

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Application

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Abstract (en)

[origin: WO0101422A1] A Built-in Self Test (BIST) scheme for testing Random Access Memories (RAMs) is disclosed. This scheme is capable of testing either stand-alone or embedded RAMs. Furthermore testing algorithms to exploit this scheme in order to detect all Neighborhood Pattern Sensitive Faults (NPSFs) as well as all cell stuck-at and transition faults in the memory array, and also all single stuck-at faults in the address decoding or the sensing/writing circuitry, are given. The BIST circuitry includes a BIST Controller, a Test Pattern Generation (TPG) unit, a register (RWR) to read and write test data from/to the memory array and a BIST I/O circuitry. The BIST Controller controls the RAM during the test mode of operation while TPG generates the proper test patterns to test the RAM. Test patterns are used to fulfill the RWR register. Since, in the proposed scheme the cells of RWR are connected directly to the sense amplifiers and write buffers of the sensing/writing circuitry, test data can be written to the cells of a word line in parallel while multiple word lines can be written with the same test data in successive write sessions. In addition various methods are given to evaluate the data retrieved in RWR from the memory array, in order to detect and locate possible faults. Finally, the BIST I/O is capable of storing test information concerning the location of a malfunction in the RAM and outputting this information to the external environment via an integrated circuit I/O port or in collaboration with a TAP controller.

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