

Title (en)  
SYNCHRONOUS CIRCUIT

Title (de)  
SYNCHRONE SCHALTUNG

Title (fr)  
CIRCUIT SYNCHRONE

Publication  
**EP 1114422 A1 20010711 (DE)**

Application  
**EP 99953713 A 19990908**

Priority  
• DE 9902845 W 19990908  
• DE 19842818 A 19980918

Abstract (en)  
[origin: DE19842818A1] A synchronous circuit (M) includes a clock input (CLKE), a clock-pulse generator (G) for generating a second clock pulse (CLKINT) locked in phase with the first clock pulse (CLKE), an input connected to the clocked input and a clock output for outputting the second clock pulse. The clock output of the generator (G) is connected to a control input of a data transmission unit (DRV) and serves to output data from, or to read data into, an integrated circuit, largely in sync with the first-clock (pulse) (CLKE). The clock-pulse generator has at least two series-connected control loops (1,2) for controlling the phase-angle of the second clock (pulse) (CLKINT). A deactivating unit (AKT) deactivated control of the first control loop (1) during transmission of data through the data transmission unit (DRV) so that control of the phase-angle of the intermediate clock (pulse) (CLKi) is interrupted.

IPC 1-7  
**G11C 7/10**; **G11C 7/22**; **G06F 13/42**

IPC 8 full level  
**G06F 1/12** (2006.01); **G06F 13/42** (2006.01); **G11C 7/10** (2006.01); **G11C 7/22** (2006.01); **G11C 11/407** (2006.01); **H03K 5/15** (2006.01); **H03L 7/00** (2006.01); **H03L 7/081** (2006.01)

CPC (source: EP KR US)  
**G06F 13/4243** (2013.01 - EP US); **G11C 7/1072** (2013.01 - EP US); **G11C 7/22** (2013.01 - EP US); **G11C 8/00** (2013.01 - KR)

Citation (search report)  
See references of WO 0017883A1

Designated contracting state (EPC)  
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DOCDB simple family (publication)  
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