Title (en)

Redundancy architecture for an interleaved memory

Title (de)

Redundanzarchitektur bei einem verschachtelten Speicher

Title (fr)

Architecture de redondance dans une mémoire entrelacée

Publication

EP 1130517 A1 20010905 (EN)

Application

EP 00830158 A 20000302

Priority

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Abstract (en)

A redundancy architecture for a memory wherein the array of memory cells is divided in at least a pair of banks or semiarrays (EVEN_BANK, ODD_BANK) singularly addressable (ADDR_latch_E, ADDR_latch_O), organized in rows and columns; the architecture comprising a certain number of packets each composed of a certain number of redundancy columns of cells (REDUNDANCY), contemplates dividing said number of packets (REDUNDANCY) in two subsets of packets (REDUNDANCY_EVEN, REDUNDANCY_ODD), each one addressable independently from the other by way of respective address circuits and providing redundancy columns of cells exclusively for a respective bank or semiarray (EVEN_BANK, ODD_BANK). <IMAGE>

IPC 1-7

G06F 11/20

IPC 8 full level

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CPC (source: EP US)

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Citation (search report)

[XA] US 5999463 A 19991207 - PARK YOUN-SIK [KR], et al

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