

Title (en)

THREE-DIMENSIONAL PACKAGING TECHNOLOGY FOR MULTI-LAYERED INTEGRATED CIRCUITS

Title (de)

DREIDIMENSIONALE VERPACKUNGSTECHNOLOGIE FÜR MEHRSCICHTIGE INTEGRIERTE SCHALTUNGEN

Title (fr)

ASSEMBLAGE TRIDIMENSIONNEL POUR CIRCUITS INTEGRES MULTICOUCHES

Publication

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Application

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US 9815477 W 19980727

Abstract (en)

[origin: WO0007240A1] Disclosed is method and apparatus (1) for packaging multilayered integrated circuit (IC) chips (2), on which logic circuits and/or memory arrays are disposed and interconnected in a novel way permitting the addressing (i.e. selection) of the logic circuits and/or arrays on these IC chip layers using a minimum number of connections and with the shortest propagation delays.

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H01L 25/065

IPC 8 full level

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