Title (en)

INTEGRATED MEMORY AND CORRESPONDING OPERATING METHOD

Title (de)

INTEGRIERTER SPEICHER UND ENTSPRECHENDES BETRIEBSVERFAHREN

Title (fr)

MEMOIRE INTEGREE ET PROCEDE POUR FAIRE FONCTIONNER CETTE DERNIERE

Publication

EP 1149382 A1 20011031 (DE)

Application

EP 00907443 A 20000125

Priority

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- DE 19903198 A 19990127

Abstract (en)

[origin: DE19903198C1] The semiconductor memory device has memory cells (MC) formed at the intersection points between word lines (WLi) and bit lines (BLi), with a differential read amplifier (SA) coupled to 3 of the bit lines via a multiplexer (MUX), allowing the difference inputs of the amplifier to be coupled to any 2 of the 3 bit lines. Complementary data can be stored in 2 memory cells coupled to the same word line, with the memory cell bit lines coupled to the difference inputs of the read amplifier via the multiplexer.

IPC 1-7

G11C 7/06; G11C 11/409

IPC 8 full level

G11C 11/401 (2006.01); **G11C 7/06** (2006.01); **G11C 7/10** (2006.01); **G11C 11/22** (2006.01)

CPC (source: EP KR US)

G11C 7/06 (2013.01 - EP US); **G11C 7/065** (2013.01 - EP US); **G11C 7/1006** (2013.01 - EP US); **G11C 11/4091** (2013.01 - KR)

Citation (search report)

See references of WO 0045392A1

Designated contracting state (EPC)

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DOCDB simple family (application)

DE 19903198 A 19990127; CN 00803218 A 20000125; DE 0000202 W 20000125; EP 00907443 A 20000125; JP 2000596570 A 20000125; KR 20017009397 A 20010726; US 91755301 A 20010727