Title (en)

Method, computer program product and apparatus for identifying splittable packets in a multithreated vliw processor

Title (de)

Verfahren, Computerprogrammprodukt und Vorrichtung zum Identifizieren von teilbaren Paketen in einem Multi-threaded VLIW Prozessor

Title (fr)

Procédé, produit de programme d'ordinateur et dispositif d'identification de paquets séparables dans un processeur multifilière vliw

Publication

**EP 1152329 A1 20011107 (EN)**

Application

**EP 01302951 A 20010329**

Priority

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Abstract (en)

A method and apparatus are disclosed for allocating functional units in a multithreaded very large instruction word (VLIW) processor. The present invention combines the techniques of conventional very long instruction word (VLIW) architectures and conventional multithreaded architectures to reduce execution time within an individual program, as well as across a workload. The present invention utilizes instruction packet splitting to recover some efficiency lost with conventional multithreaded architectures. Instruction packet splitting allows an instruction bundle to be partially issued in one cycle, with the remainder of the bundle issued during a subsequent cycle. There are times, however, when instruction packets cannot be split without violating the semantics of the instruction packet assembled by the compiler. A packet split identification bit is disclosed that allows hardware to efficiently determine when it is permissible to split an instruction packet. The split bit informs the hardware when splitting is prohibited. The allocation hardware assigns as many instructions from each packet as will fit on the available functional units, rather than allocating all instructions in an instruction packet at one time, provided the split bit has not been set. Those instructions that cannot be allocated to a functional units are retained in a ready-to-run register. On subsequent cycles, instruction packets in which all instructions have been issued to functional units are updated from their thread's instruction stream, while instruction packets with instructions that have been held are retained. The functional unit allocation logic can then assign instructions from the newly-loaded instruction packets as well as instructions that were not issued from the retained instruction packets. <IMAGE>

IPC 1-7

**G06F 9/38**

IPC 8 full level

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Citation (search report)

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