Title (en)
Applicative multiprocessor interface, not needing the use of a multiprocessor operating system

Title (de)
Applikative Multiprozessorschnittstelle, die kein Multiprozessorbetriebssystem braucht

Title (fr)
Interface applicative multiprocesseur, ne nécessitant pas l'utilisation d'un système d'exploitation multiprocesseur

Publication
EP 1156418 A1 20011121 (FR)

Application
EP 01401251 A 20010515

Priority
FR 0006286 A 20000517

Abstract (en)
Method for executing a sequence of instructions simultaneously on several processors (3,4,5) of a multiprocessor machine: stage 1, a single processor operating system is launched on a first processor (2); stage 2, the first processor (2) at least controls another processor (3), called application processor, of the machine, for the execution of one or more instruction sequences (17,18,19) under the control of the first processor. The second stage includes: (a) a first phase (10) in which the first processor (2) loads, to a first address (A1) of a common memory zone (20), a first sequence of instructions (21) executable by the application processors (3,4,5) for self initializing. It sends to a second address (A2) of the common memory zone a second sequence of instructions (17) executable by the application processors after initialization; a second phase (11) in which the first processor constructs in the common memory zone, by searching micro-logical tables for machine configuration, an application table (16) with lines each accessible by an identifier for the application processor containing the second address; a third phase (12) in which the first processor searches in a micro-logical application processor starting table (28) for the first address; a fourth stage (13) in which the first processor sends an interrupt (25,26,27) to at least an application processor which causes a rerouting of the application processor to the first address (A1) contained in the micro-logical table (28) so that the application processor executes the first sequence of instructions (21) at the end of which the application processor is routed to the second address (A2) contained in the line of the application table (16) accessible by the identifier of the application processor

IPC 1-7
G06F 9/445

IPC 8 full level
G06F 11/28 (2006.01); **G06F 9/445** (2006.01); **G06F 15/177** (2006.01)

CPC (source: EP US)
G06F 9/4403 (2013.01 - EP US); **G06F 9/4405** (2013.01 - EP US); **G06F 11/3672** (2013.01 - EP US); **G06F 15/177** (2013.01 - EP US)

Citation (search report)
- [XYA] EP 0335812 A2 19891004 - IBM [US]
- [XA] US 5867703 A 19990202 - MILLER DAVID A [US], et al
- [A] US 5687073 A 19971111 - KISHIMOTO KUNIYUKI [JP]
- [Y] CORSINI P ET AL: "MULTIBUG: INTERACTIVE DEBUGGING IN DISTRIBUTED SYSTEMS", IEEE MICRO,US,IEEE INC. NEW YORK, vol. 6, no. 3, 1 June 1986 (1986-06-01), pages 26 - 33, XP000719945, ISSN: 0272-1732

Designated contracting state (EPC)
DE FR GB IT

DOCDB simple family (publication)
EP 1156418 A1 20011121; **EP 1156418 B1 20190220**; FR 2809204 A1 20011123; FR 2809204 B1 20030919; JP 2002007361 A 20020111; US 2001044913 A1 20011122; US 2005015749 A1 20050120; US 6928539 B2 20050809; US 7574696 B2 20090811

DOCDB simple family (application)
EP 01401251 A 20010515; FR 0006286 A 20000517; JP 2001146297 A 20010516; US 85849001 A 20010517; US 91749904 A 20040813