

Title (en)

FULL PAGE INCREMENT/DECREMENT BURST FOR DDR SDRAM/SGRAM

Title (de)

AUF- UND ABZAHLENDER BURSTZUGRIFF MIT VOLLSTÄNDIGEM SEITENMODUS FÜR DDR SDRAM/SGRAMS

Title (fr)

RAFALE D'INCREMENT/DECREMENT PLEINE PAGE POUR UNE MEMOIRE SDRAM/SGRAM A DOUBLE DEBIT BINAIRE

Publication

**EP 1157387 B1 20030910 (EN)**

Application

**EP 00911960 A 20000225**

Priority

- US 0004761 W 20000225
- US 25903499 A 19990226

Abstract (en)

[origin: WO051132A1] A dual-data rate (DDR) synchronous dynamic random access memory (SDRAM)/synchronous graphic random access memory (SGRAM), having a full-page increment/decrement burst mode. In one embodiment, the DDR SDRAM/SGRAM includes a memory array and a logic circuitry coupled thereto. The memory array is addressable by even and odd word addresses. The logic circuitry has a burst increment mode to access the array starting at an even word address and a burst decrement mode to access the array starting at an odd word address.

IPC 1-7

**G11C 7/10**

IPC 8 full level

**G11C 7/10** (2006.01); **G11C 8/12** (2006.01); **G11C 11/408** (2006.01)

CPC (source: EP KR US)

**G11C 7/1018** (2013.01 - EP US); **G11C 7/103** (2013.01 - EP US); **G11C 7/1042** (2013.01 - EP US); **G11C 7/1045** (2013.01 - EP US); **G11C 7/1066** (2013.01 - EP US); **G11C 7/1072** (2013.01 - EP US); **G11C 8/12** (2013.01 - EP US); **G11C 11/407** (2013.01 - KR); **G11C 11/408** (2013.01 - EP US)

Designated contracting state (EPC)

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