

Title (en)
Shared communication bus arbitration system and method for arbitrating

Title (de)
Arbitrierungssystem für einen verteilten Übertragungsbus und Arbitrierungsverfahren

Title (fr)
Système d'arbitrage d'un bus de communication partagé et méthode d'arbitrage

Publication
EP 1174798 A2 20020123 (EN)

Application
EP 01122637 A 19970627

Priority
• EP 97933270 A 19970627
• US 67122196 A 19960627

Abstract (en)
A parallel packetized intermodule arbitrated high speed control data bus system which allows high speed communications between microprocessor modules in a more complex digital processing environment. The system features a simplified hardware architecture featuring fast FIFO queuing operating at 12.5 MHz, TTL CMOS compatible level clocking signals, single bus master arbitration, synchronous clocking, DMA, and unique module addressing for multiprocessor systems. The system includes a parallel data bus with sharing bus masters residing on each processing module decreeing the communication and data transfer protocols. Bus arbitration is performed over a dedicated serial arbitration line and each requesting module competes for access to the parallel data bus by placing the address of the requesting module on the arbitration line and monitoring the arbitration line for collisions. <IMAGE>

IPC 8 full level
G06F 13/376 (2006.01); **G06F 13/374** (2006.01); **H04B 1/7075** (2011.01); **H04B 1/708** (2011.01)

CPC (source: EP KR US)
G06F 13/374 (2013.01 - EP KR US); **G06F 13/376** (2013.01 - EP US); **H04B 1/7075** (2013.01 - EP US); **H04B 1/70753** (2013.01 - EP US); **H04B 1/70755** (2013.01 - EP US); **H04B 1/70758** (2013.01 - EP US); **H04B 1/708** (2013.01 - EP US); **H04B 2201/70702** (2013.01 - EP US)

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