

Title (en)
MEMORY CELL ARRANGEMENT AND METHOD FOR PRODUCING SAME

Title (de)
SPEICHERZELLENANORDNUNG UND VERFAHREN ZU DEREN HERSTELLUNG

Title (fr)
DISPOSITIF MEMOIRE ET PROCEDE DE FABRICATION ASSOCIE

Publication
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Application
EP 00929252 A 20000327

Priority
• DE 0000932 W 20000327
• DE 19914490 A 19990330

Abstract (en)
[origin: DE19914490C1] A memory cell array, comprising trench conductive structures and upper source/drain regions which overlap over a large area to provide low contact resistance between a capacitor and a transistor, is new. A memory cell array comprises (a) a substrate (1) with intersecting first and second trenches (G1); (b) a transistor upper source/drain region (S/Do) formed in the substrate adjacent two first trenches (G1) and two second trenches; (c) a transistor lower source/drain region located below the upper source/drain region (S/Do); (d) conductive structures (L) located in the first trenches (G1) between the second trenches, each conductive structure adjoining one of the upper source/drain regions (S/Do) at a respective first side wall of the associated first trench and being insulated from the second side wall and the bottom of the first trench (G1) by an insulating structure (I); (e) a word line (W) extending parallel to the first trenches (G1) and having cuffs extending into the second trenches, the word line (W) being arranged over an insulating layer (I2) between the second trenches and located above the upper source/drain region (S/Do); (f) a further insulating layer (I3) arranged on the word line (W) and insulating spacers (Sp) adjacent the sides of the word line (W); and (g) a capacitor connected to the upper source/drain region (S/Do) by a contact (K) which is arranged on the conductive structure (L) and between word lines (W). An Independent claim is also included for production of the above memory cell array.

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