

Title (en)

APPARATUS AND METHOD FOR A PROGRAMMABLE SECURITY PROCESSOR

Title (de)

VORRICHTUNG UND VERFAHREN FÜR EINEN PROGRAMMIERBAREN SICHERHEITS-PROZESSOR

Title (fr)

APPAREIL ET PROCEDE POUR UN PROCESSEUR DE SECURITE PROGRAMMABLE

Publication

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Application

EP 00932153 A 20000505

Priority

- US 0012479 W 20000505
- US 13313199 P 19990507

Abstract (en)

[origin: WO0068791A1] A digital logic circuit having a programmable security circuit which stores a set of authorized configuration security keys (538). The security circuit compares authorization configuration keys (360) with incoming configuration request, and selectively enables a new configuration (544) for the programmable logic device.

IPC 1-7

G06F 11/00; **G06F 12/02**; **G06F 11/30**

IPC 8 full level

G06F 12/14 (2006.01); **G06F 21/76** (2013.01); **H04L 9/08** (2006.01)

CPC (source: EP KR)

G06F 11/00 (2013.01 - KR); **G06F 21/76** (2013.01 - EP); **G06F 2207/7219** (2013.01 - EP)

Citation (search report)

- [A] EP 0895164 A2 19990203 - MOTOROLA INC [US]
- [X] MIRSKY E ET AL: "MATRIX: a reconfigurable computing architecture with configurable instruction distribution and deployable resources", FPGAS FOR CUSTOM COMPUTING MACHINES, 1996. PROCEEDINGS. IEEE SYMPOSIUM ON NAPA VALLEY, CA, USA 17-19 APRIL 1996, LOS ALAMITOS, CA, USA,IEEE COMPUT. SOC, US, 17 April 1996 (1996-04-17), pages 157 - 166, XP010206378, ISBN: 978-0-8186-7548-5
- [X] RUPP C R ET AL: "The NAPA adaptive processing architecture", FPGAS FOR CUSTOM COMPUTING MACHINES, 1998. PROCEEDINGS. IEEE SYMPOSIUM ON NAPA VALLEY, CA, USA 15-17 APRIL 1998, LOS ALAMITOS, CA, USA,IEEE COMPUT. SOC, US, 15 April 1998 (1998-04-15), pages 28 - 37, XP010298175, ISBN: 978-0-8186-8900-0
- See references of WO 0068791A1

Designated contracting state (EPC)

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