Title (en)
METHOD AND APPARATUS FOR LOOSE REGISTER ENCODING WITHIN A PIPELINED PROCESSOR

Title (de)
VERFAHREN UND VORRICHTUNG ZUR LOCKERER REGISTERKODIERUNG IN PIPELINEPROZESSOR

Title (fr)
PROCEDE ET APPAREIL D'ENCODAGE DE REGISTRE LIBRE DANS UN PROCESSEUR PIPELINE

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Abstract (en)
[origin: WO0070446A2] An improved method and apparatus for implementing instructions in a pipelined central processing unit (CPU) or user-customizable microprocessor. In a first aspect of the invention, an improved method of "loosely" encoding register numbers to indicate register immediate data operand usage is disclosed. One embodiment comprises instruction words having multi-bit data fields defined therein which encode various types of immediate operands. Such multi-bit field definitions provide the programmer with additional flexibility in performing a variety of operations, including non-commutative operations. A method of synthesizing a processor design incorporating the aforementioned "loose" register encoding is also disclosed. Exemplary gate logic synthesized using the aforementioned method, and a computer program and system capable of implementing these methods are further disclosed.

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