

Title (en)
Multilayer circuit board and method of manufacturing the same

Title (de)
Mehrschichtige Leiterplatte und Verfahren zu deren Herstellung

Title (fr)
Panneau à circuit multicouches et son procédé de fabrication

Publication
EP 1209959 A3 20040310 (EN)

Application
EP 01126948 A 20011113

Priority
• JP 2000360220 A 20001127
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Abstract (en)
[origin: EP1209959A2] A molded interconnect device (MID) having a multilayer circuit of a reduced thickness, in which a layer-to-layer connection(s) is formed with high reliability, is provided as a multilayer circuit board. The multilayer circuit board comprises a substrate (10) having a first surface (14) and a second surface (15) extending from an end of the first surface (14) at a required angle relative to the first surface (14), and the multilayer circuit formed on the first surface (14) and composed of a plurality of circuit layers. Each of the circuit layers is provided with a conductive layer (20,22,24,26) having a required circuit pattern and an insulation layer (30,32,34) formed on the conductive layer by film formation. The layer-to-layer connection of the multilayer circuit is made through a second conductive layer (20) formed on the second surface (15) of the substrate. <IMAGE>

IPC 1-7
H05K 3/46

IPC 8 full level
H05K 3/46 (2006.01); **H05K 1/11** (2006.01); **H05K 1/18** (2006.01); **H05K 3/40** (2006.01); **H05K 1/00** (2006.01); **H05K 3/00** (2006.01); **H05K 3/02** (2006.01)

CPC (source: EP KR US)
H05K 1/119 (2013.01 - EP US); **H05K 1/183** (2013.01 - EP US); **H05K 3/403** (2013.01 - EP US); **H05K 3/46** (2013.01 - KR); **H05K 3/4697** (2013.01 - EP US); **B29L 2031/3493** (2013.01 - EP US); **H05K 1/0284** (2013.01 - EP US); **H05K 3/027** (2013.01 - EP US); **H05K 3/4644** (2013.01 - EP US); **H05K 2201/09036** (2013.01 - EP US); **H05K 2201/09045** (2013.01 - EP US); **H05K 2201/09118** (2013.01 - EP US); **H05K 2201/0919** (2013.01 - EP US); **H05K 2201/09645** (2013.01 - EP US); **Y10T 29/49155** (2015.01 - EP US)

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