

Title (en)

Circuit and method for hardware-assisted software flushing of data and instruction caches

Title (de)

Schaltung und Verfahren zur Hardware-unterstützten Software-Räumung von Daten- und Befehls cachespeichern

Title (fr)

Circuit et procédé d'invalidation par logiciel d'antémémoires d'instructions et données assistés par matériel

Publication

EP 1220100 A3 20031008 (EN)

Application

EP 01310596 A 20011219

Priority

US 75137100 A 20001229

Abstract (en)

[origin: EP1220100A2] A cache flush controller, and an associated method, selectably flushes a memory cache of a data processor. The cache flush controller operates at a memory bus level of the data processor and operates to flush a selected line, or lines of the memory cache by writing arbitrary, selected values to the selected line or lines of the memory cache. <IMAGE>

IPC 1-7

G06F 12/08

IPC 8 full level

G06F 12/08 (2006.01)

CPC (source: EP US)

G06F 12/0891 (2013.01 - EP US)

Citation (search report)

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- [X] US 5363496 A 19941108 - KATO RIKAKO [JP], et al
- [A] EP 0332303 A2 19890913 - IBM [US]
- [YA] MARGULIS N: "I860 MICROPROCESSOR INTERNAL ARCHITECTURE", MICROPROCESSORS AND MICROSYSTEMS, IPC BUSINESS PRESS LTD. LONDON, GB, vol. 14, no. 2, 1 March 1990 (1990-03-01), pages 89 - 96, XP000102966, ISSN: 0141-9331
- [A] BANNON P ET AL: "INTERNAL ARCHITECTURE OF ALPHA 21164 MICROPROCESSOR", DIGEST OF PAPERS OF THE COMPUTER SOCIETY COMPUTER CONFERENCE (SPRING) COMPCON. TECHNOLOGIES FOR THE INFORMATION SUPERHIGHWAY. SAN FRANCISCO, MAR. 5 - 9, 1995, LOS ALAMITOS, IEEE COMP. SOC. PRESS, US, vol. CONF. 40, 5 March 1995 (1995-03-05), pages 79 - 87, XP000545418, ISBN: 0-7803-2657-1

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CN113168293A

Designated contracting state (EPC)

AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR

DOCDB simple family (publication)

EP 1220100 A2 20020703; EP 1220100 A3 20031008; EP 1220100 B1 20080813; CA 2366351 A1 20020629; DE 60135301 D1 20080925; US 2002087799 A1 20020704; US 6691210 B2 20040210

DOCDB simple family (application)

EP 01310596 A 20011219; CA 2366351 A 20011221; DE 60135301 T 20011219; US 75137100 A 20001229