Title (en)

Magnetic random access memory

Title (de)

Magnetischer Direktzugriffspeicher

Title (fr)

Mémoire magnétique à accès aléatoire

Publication

EP 1225591 A2 20020724 (EN)

Application

EP 01126566 A 20011115

Priority

JP 2000395723 A 20001226

Abstract (en)

A bias voltage generating circuit (21) includes a series circuit of a magneto-resistance element (Rref) and a MOS transistor (QN3). The MR ratio of the magneto-resistance element (Rref) in the series circuit is set to 1/2 the MR ratio of the magneto-resistance element in a memory cell. An adjusting resistor (r) has a resistance value 1/2 the interconnection resistance of a bit line. A bias voltage generating circuit (21) applies a bias voltage (Vbias) to a sense current source. When a constant current flows in the bias voltage generating circuit (21), the sense current source supplies a sense current equal to the constant current to a bit line.

IPC 1-7

G11C 11/16

IPC 8 full level

G11C 11/14 (2006.01); **G11C 11/15** (2006.01); **G11C 11/16** (2006.01); **H01L 21/8246** (2006.01); **H01L 27/105** (2006.01); **H01L 43/08** (2006.01)

CPC (source: EP KR US)

G11C 7/065 (2013.01 - EP US); **G11C 11/15** (2013.01 - KR); **G11C 11/16** (2013.01 - EP US); **G11C 11/161** (2013.01 - EP US); **G11C 11/1655** (2013.01 - EP US); **G11C 11/1673** (2013.01 - EP US)

Citation (examination)

WO 0008650 A1 20000217 - MOTOROLA INC [US]

Cited by

DE10228560B4; US6990024B2; US9087579B1; WO2015103516A1

Designated contracting state (EPC)

DE FR GB

DOCDB simple family (publication)

US 2002080644 A1 20020627; **US 6504752 B2 20030107**; CN 1197084 C 20050413; CN 1362709 A 20020807; EP 1225591 A2 20020724; EP 1225591 A3 20030423; JP 2002197853 A 20020712; JP 3920565 B2 20070530; KR 100465663 B1 20050113; KR 20020071445 A 20020912; TW 541526 B 20030711

DOCDB simple family (application)

US 98798001 A 20011116; CN 01143918 A 20011226; EP 01126566 A 20011115; JP 2000395723 A 20001226; KR 20010083981 A 20011224; TW 90129999 A 20011204