Title (en)

Clock synchronizing circuit

Title (de)

Taktsynchronisationsschaltung

Title (fr)

Circuit de synchronisation d'horloge

Publication

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Application

EP 02250344 A 20020118

Priority

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Abstract (en)

A clock synchronizing circuit of the present invention includes a first AID (Analog-to-Digital) converter for converting a first-channel baseband signal, which is subjected to orthogonal detection together with a second-channel baseband signal, to a first digital signal. A second A/D converter converts the second-channel baseband signal to a second digital signal. A controller controls the sampling phase of the second A/D converter on the basis of the first digital signal. A detector detects a shift of the sampling phase of the second digital signal relative to the first channel. An interpolator interpolates the second digital signal in accordance with a coefficient based on the shift of the sampling phase detected by the detector. Even when two channels of baseband circuits are different in electric length, the interpolator automatically, digitally cancels the difference. The circuit therefore prevents a BER (Bit Error Rate) characteristic from being degraded. <IMAGE>

IPC 1-7

H04L 7/02

IPC 8 full level

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