

Title (en)  
SYSTEMS AND METHODS FOR HOLDOVER CIRCUITS IN PHASE LOCKED LOOPS

Title (de)  
SYSTEME UND VERFAHREN FÜR EINE SCHALTUNG ZUM AUFRECHTERHALTEN DER FREQUENZ IN PHASENREGELSCHLEIFEN

Title (fr)  
SYSTEMES ET PROCEDES RELATIFS A DES CIRCUITS DE MAINTIEN DANS DES BOUCLES A PHASE ASSERVIE

Publication  
**EP 1228567 A2 20020807 (EN)**

Application  
**EP 00988481 A 20001024**

Priority  
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Abstract (en)  
[origin: WO0131792A2] Phase locked loops are described which handle momentary breaks in an input communication channel. The phase locked loops provide the capability to "hold" the output clock in a communication system at or very near the last output frequency before the loss of input data. The phase locked loops according to the teachings of the present invention include a differential phase detector that receives an input signal and feedback signal and produces a different output signal. An electronic selector circuit is coupled to a differential output of the phase detector with an input that is responsive to a detected state of the input signal. An operational amplifier based loop filter circuit is provided in the phased locked loop. The electronic selector circuit provides the differential output of the phase detector at a pair of inputs to the operational amplifier. A voltage controlled oscillator is coupled to an output of the operational amplifier and provides an output frequency for the phased locked loop circuit. The electronic selector circuit is operable to control the input to the operational amplifier to hold an output frequency of the voltage controlled oscillator at a substantially constant frequency.  
[origin: WO0131792A2] Phase locked loops are described which handle momentary break in an input communication channel. The phase locked loops provide the capability to "hold" the output clock in a communication system at or very near the last output frequency before the loss of input data. The phase locked loops according to the teachings of the present invention include a differential phase detector that receives an input signal and feedback signal and produces a different output signal. An electronic selector circuit is coupled to a differential output of the phase detector with an input that is responsive to a detected state of the input signal. An operational amplifier based loop filter circuit is provided in the phased locked loop. The electronic selector circuit provides the differential output of the phase detector at a pair of inputs to the operational amplifier. A voltage controlled oscillator is coupled to an output of the operational amplifier and provides an output frequency for the phased locked loop circuit. The electronic selector circuit is operable to control the input to the operational amplifier to hold an output frequency of the voltage controlled oscillator at a substantially constant frequency.

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