

Title (en)
SYSTEMS AND METHODS FOR HOLDOVER CIRCUITS IN PHASE LOCKED LOOPS

Title (de)
SYSTEME UND VERFAHREN FÜR EINE SCHALTUNG ZUM AUFRECHTERHALTEN DER FREQUENZ IN PHASENREGELSCHLEIFEN

Title (fr)
SYSTEMES ET PROCEDES RELATIFS A DES CIRCUITS DE MAINTIEN DANS DES BOUCLES A PHASE ASSERVIE

Publication
EP 1228567 A2 20020807 (EN)

Application
EP 00988481 A 20001024

Priority
• US 0041471 W 20001024
• US 43202299 A 19991029

Abstract (en)
[origin: WO0131792A2] Phase locked loops are described which handle momentary breaks in an input communication channel. The phase locked loops provide the capability to "hold" the output clock in a communication system at or very near the last output frequency before the loss of input data. The phase locked loops according to the teachings of the present invention include a differential phase detector that receives an input signal and feedback signal and produces a different output signal. An electronic selector circuit is coupled to a differential output of the phase detector with an input that is responsive to a detected state of the input signal. An operational amplifier based loop filter circuit is provided in the phased locked loop. The electronic selector circuit provides the differential output of the phase detector at a pair of inputs to the operational amplifier. A voltage controlled oscillator is coupled to an output of the operational amplifier and provides an output frequency for the phased locked loop circuit. The electronic selector circuit is operable to control the input to the operational amplifier to hold an output frequency of the voltage controlled oscillator at a substantially constant frequency.
[origin: WO0131792A2] Phase locked loops are described which handle momentary break in an input communication channel. The phase locked loops provide the capability to "hold" the output clock in a communication system at or very near the last output frequency before the loss of input data. The phase locked loops according to the teachings of the present invention include a differential phase detector that receives an input signal and feedback signal and produces a different output signal. An electronic selector circuit is coupled to a differential output of the phase detector with an input that is responsive to a detected state of the input signal. An operational amplifier based loop filter circuit is provided in the phased locked loop. The electronic selector circuit provides the differential output of the phase detector at a pair of inputs to the operational amplifier. A voltage controlled oscillator is coupled to an output of the operational amplifier and provides an output frequency for the phased locked loop circuit. The electronic selector circuit is operable to control the input to the operational amplifier to hold an output frequency of the voltage controlled oscillator at a substantially constant frequency.

IPC 1-7
H03L 7/14

IPC 8 full level
H03L 7/14 (2006.01); **H04J 3/06** (2006.01); **H04L 7/00** (2006.01); **H04L 7/033** (2006.01)

CPC (source: EP US)
H03L 7/14 (2013.01 - EP US); **H04J 3/0688** (2013.01 - EP US); **H04L 7/0083** (2013.01 - EP US); **H04L 7/033** (2013.01 - EP US)

Citation (search report)
See references of WO 0131792A2

Cited by
US9660797B2

Designated contracting state (EPC)
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

DOCDB simple family (publication)
WO 0131792 A2 20010503; WO 0131792 A3 20020103; WO 0131792 A9 20020207; AT E313876 T1 20060115; AU 2468701 A 20010508; BR 0015159 A 20020716; CA 2389295 A1 20010503; CA 2389295 C 20050125; CN 1187899 C 20050202; CN 1413384 A 20030423; DE 60025029 D1 20060126; DE 60025029 T2 20060803; EP 1228567 A2 20020807; EP 1228567 B1 20051221; ES 2256084 T3 20060716; MX PA02004269 A 20030128; US 7010076 B1 20060307

DOCDB simple family (application)
US 0041471 W 20001024; AT 00988481 T 20001024; AU 2468701 A 20001024; BR 0015159 A 20001024; CA 2389295 A 20001024; CN 00817757 A 20001024; DE 60025029 T 20001024; EP 00988481 A 20001024; ES 00988481 T 20001024; MX PA02004269 A 20001024; US 43202299 A 19991029