Title (en)

SYSTEM AND METHOD TO IMPLEMENT A CROSS-BAR SWITCH OF A BROADBAND PROCESSOR

Title (de)

SYSTEM UND VERFAHREN ZUM IMPLEMENTIEREN EINES CROSS-BARSCHALTERS EINES BREITBANDPROZESSORS

Title (fr)

SYSTEME ET PROCEDE DE MISE EN OEUVRE DE COMMUTATEUR CROSSBAR DE PROCESSEUR LARGE BANDE

Publication

EP 1236090 A4 20020904 (EN)

Application

EP 00910150 A 20000211

Priority

- US 0003566 W 20000211
- US 11984199 P 19990212
- US 38240299 A 19990824

Abstract (en)

[origin: WO0048070A1] The present invention provides a cross-bar circuit (100) that implements a switch (115) of a broadband processor. The cross-bar circuit (100) includes: a switch circuit (115) which includes 2<m>.2<n>:1 multiplexor circuits (202-204) where each of the 2<n>:1 multiplexor circuits (202-204) has a unique n-bit index input, one disable input, and a 2<n>-bit wide source input receives an n-bit index at the n-bit index input, a disable bit at the disable input, and the 2<n>-bit input source word at the 2<n>-bit wide source input, and decodes the n-bit index either to select and output as an output destination bit one bit from the 2<n>-bit input source word if the disable bit has a logic low value; a cache memory (110) that has 2<m> cache datapath inputs; and 2<m> cache index input; and a control circuit (105) that has a plurality of control inputs receives the partially decoded instruction information on the plurality of control inputs, provides a second set of the n-bit indexes for the switch circuit (115), and provides the disable bits for the switch circuit (115) where the control circuit (105) is logically coupled to the switch circuit (115) and to the cache memory (110).

IPC 1-7

G06F 9/30

IPC 8 full level

G06F 7/76 (2006.01); **G06F 9/308** (2006.01)

CPC (source: EP)

G06F 7/76 (2013.01); **G06F 9/30018** (2013.01)

Citation (search report)

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- [A] US 5367694 A 19941122 - UENO KIYOJI [JP]
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- See references of WO 0048070A1

Designated contracting state (EPC)

AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

DOCDB simple family (publication)

WO 0048070 A1 20000817; EP 1236090 A1 20020904; EP 1236090 A4 20020904

DOCDB simple family (application)

US 0003566 W 20000211; EP 00910150 A 20000211