Title (en)
GLOBAL BUS SYNCHRONOUS TRANSACTION ACKNOWLEDGE WITH NONRESPONSE DETECTION

Title (de)
GLOBALE BUS-SYNCHRONE BESTÄTIGUNG EINER TRANSAKTION MIT ERKENNUNG DES FEHLERS EINER ANTWORT

Title (fr)
ACCUSE DE RECEPTION DE TRANSACTION SYNCHRONE DE BUS GLOBAL AVEC DETECTION DE NON-REPONSE

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Application
EP 00923146 A 20000406

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Abstract (en)
[origin: WO0060462A1] An integrated multi-processor system with clusters (130, 131, 132, 133) of processors (25) on a high speed split transaction bus (16) uses a transaction acknowledge (TACK), by a target device in response to receiving a request from a master device on the bus. The master and target devices connect to the bus via a global bus interface (17; 31B, 33B) with FIFO registers (31A, 33A) acting as buffers, and the target interface includes a TACK generator (Fig. 6) that flips the state of the global bus' TACK line (TACK#) upon determining that a broadcast request is addressed to its target device. A bus idle default device (BIDD) (18; Fig. 8) generates a TACK signal when no device is on the bus, and also detects the absence of any TACK response (165) by monitoring the state of the TACK line, thereby indicating that a master device attempted to address a nonexistent target device. The BIDD then generates a dummy response for the requesting master device with data flags set to invalid data.

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