Title (en)

Power optimized input circuit

Title (de)

Leistungsoptimierte Eingangsschaltung

Title (fr)

Circuit d'entrée optimisé en puissance électrique

Publication

EP 1261120 B1 20041201 (DE)

Application

EP 02360135 A 20020429

Priority

DE 10125283 A 20010523

Abstract (en)

[origin: EP1261120A1] The arrangement has a first current source (ST1), a unit for electrical isolation, an intermediate resistance (RZ) and a second current source (ST2). The unit for electrical isolation and the intermediate resistance are both connected between the two current sources. Each current source contains a transistor (T1,T2), a resistor (RS1,RS2) and a Zener diode (S1,S2). AN Independent claim is also included for a parallel input/output unit for railway signaling.

IPC 1-7

H02M 3/155; G05F 3/18; B60M 3/02

IPC 8 full level

B60M 3/02 (2006.01); **G05F 3/18** (2006.01); **H02M 3/155** (2006.01)

CPC (source: EP)

G05F 3/18 (2013.01)

Cited by

US2019199331A1; EP3503399A1; CN109962700A; JP2019115045A; US10826472B2

Designated contracting state (EPC)

AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR

DOCDB simple family (publication)

EP 1261120 A1 20021127; **EP 1261120 B1 20041201**; AT E284087 T1 20041215; DE 10125283 A1 20021128; DE 50201652 D1 20050105

DOCDB simple family (application)

EP 02360135 A 20020429; AT 02360135 T 20020429; DE 10125283 A 20010523; DE 50201652 T 20020429