

Title (en)

CIRCUIT AND METHOD FOR EVALUATING CAPACITORS IN MATRICES

Title (de)

SCHALTUNGSANORDNUNG UND VERFAHREN ZUM BEWERTEN VON KAPAZITÄTEN IN MATRIZEN

Title (fr)

ENSEMBLE DE CIRCUITS ET PROCEDE POUR EVALUER DES CONDENSATEURS DANS DES MATRICES

Publication

EP 1264190 A1 20021211 (DE)

Application

EP 01913677 A 20010216

Priority

- DE 0100626 W 20010216
- DE 10010888 A 20000306

Abstract (en)

[origin: DE10010888A1] The capacitance evaluation circuit has a test path (2) coupled to one electrode of each capacitance (Cchar) to be measured, for providing 2 different potentials (V1,V2) and a measuring path (3) coupled to the other electrode of the capacitance, having 2 parallel arms coupled to a common potential (V0), one of which contains a measuring instrument for evaluation of the capacitance. A control device allows each individual capacitance to be measured to be coupled to the 2 different potentials, using integrated switching transistors (T5,T6,T7,T8), using signals provided by an address decoder (10,11).

IPC 1-7

G01R 27/26

IPC 8 full level

G11C 7/06 (2006.01); **G11C 11/405** (2006.01); **G11C 11/4091** (2006.01)

CPC (source: EP KR US)

G01R 27/26 (2013.01 - KR); **G11C 7/06** (2013.01 - EP US); **G11C 11/405** (2013.01 - EP US); **G11C 11/4091** (2013.01 - EP US); **G11C 2207/063** (2013.01 - EP US)

Citation (search report)

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