Title (en)

TILED GRAPHICS ARCHITECTURE

Title (de)

FLIESENARTIGABBILDUNGSARCHITEKTUR

Title (fr)

ARCHITECTURE GRAPHIQUE EN MOSAIQUES

Publication

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Application

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Abstract (en)

[origin: WO0175804A1] A method and apparatus for reducing memory bandwidth utilization in a tiled graphics architecture is disclosed. In one embodiment, a microprocessor reads vertex data for a graphics primitive from graphics memory. The processor determines with which bins the graphics primitive intersects. Assuming that the processor determines that the graphics primitive intersects a first and a second bin, the processor writes the vertex data for the graphics primitve to a first bin storage area in graphics memory. The processor then writes a pointer to a second bin storage area. The pointer indicates the location in memory of the actual vertex data.

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IPC 8 full level

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