Title (en)

MULTI-FINGER CURRENT BALLASTING ESD PROTECTION CIRCUIT AND INTERLEAVED BALLASTING FOR ESD-SENSITIVE CIRCUITS

Title (de)

MEHRFINGER-STROMBALLAST-ESD-SCHUTZSCHALTUNG UND VERSCHACHTELTES BALLASTVERFAHREN FÜR ESD-EMPFINDLICHE SCHALTUNGEN

Title (fr)

CIRCUIT DE PROTECTION CONTRE DES DECHARGES ELECTROSTATIQUES, COMPRENANT DES RESISTANCES DE PROTECTION ET DES LAMELLES CONDUCTRICES

Publication

EP 1299932 A4 20060426 (EN)

Application

EP 01948390 A 20010615

Priority

- US 0119213 W 20010615
- US 21173500 P 20000615
- US 21451300 P 20000628
- US 26300501 P 20010119
- US 27215901 P 20010228
- US 27556301 P 20010314
- US 28155201 P 20010404
- US 28435601 P 20010417
- US 88142201 A 20010614

Abstract (en)

[origin: WO0197358A1] A multi-finger electrostatic discharge (ESD) protection circuit has at least two first resistive channels (RS1, RS2) defining input fingers. At least two field effect transistors (908, 906), each having a drain and source are connected to corresponding ones of the at least two input fingers. The gate terminals of at least one of the at least two FETs are configured to be biased by an ESD potential applied to the drain electrodes to reduce the turn-on potential of the ESD device. At least two second resistive channels are connected between a corresponding one of the source terminals of the at least two FETs and a circuit return path.

IPC 8 full level

H01L 27/04 (2006.01); **H02H 9/00** (2006.01); **H01L 21/822** (2006.01); **H01L 21/8234** (2006.01); **H01L 27/02** (2006.01); **H01L 27/06** (2006.01); **H01L 27/088** (2006.01)

CPC (source: EP KR)

H01L 27/027 (2013.01 - EP); **H01L 27/0281** (2013.01 - EP); **H01L 27/04** (2013.01 - KR)

Citation (search report)

- [YA] EP 0851552 A1 19980701 - SGS THOMSON MICROELECTRONICS [IT]
- [XA] US 5468667 A 19951121 - DIAZ CARLOS H [US], et al
- [XAY] US 4825280 A 19890425 - CHEN KUEING L [US], et al
- [Y] US 4763184 A 19880809 - KRIEGER GADI [US], et al
- [XA] US 4845536 A 19890704 - HEINECKE GUENTER [DE], et al
- [A] POLGREEN T L ET AL: "IMPROVING THE ESD FAILURE THRESHOLD OF SILICIDED N-MOS OUTPUT TRANSISTORS BY ENSURING UNIFORM CURRENT FLOW", IEEE TRANSACTIONS ON ELECTRON DEVICES, IEEE SERVICE CENTER, PISACATAWAY, NJ, US, vol. 39, no. 2, 1 February 1992 (1992-02-01), pages 379 - 388, XP000247214, ISSN: 0018-9383
- See references of WO 0197358A1

Designated contracting state (EPC)

DE FR GB NL

DOCDB simple family (publication)

WO 0197358 A1 20011220; EP 1299932 A1 20030409; EP 1299932 A4 20060426; JP 2004521477 A 20040715; JP 4942278 B2 20120530; KR 20030019432 A 20030306

DOCDB simple family (application)

US 0119213 W 20010615; EP 01948390 A 20010615; JP 2002511451 A 20010615; KR 20027017113 A 20021214