

Title (en)

SEMICONDUCTOR MEMORY CELL ARRANGEMENT AND METHOD FOR PRODUCING THE SAME

Title (de)

HALBLEITERSPEICHER-ZELLENANORDNUNG UND VERFAHREN ZU DEREN HERSTELLUNG

Title (fr)

AGENCEMENT DE CELLULES DE MEMOIRE A SEMICONDUCTEURS ET SON PROCEDE DE REALISATION

Publication

EP 1305827 A1 20030502 (DE)

Application

EP 01956376 A 20010723

Priority

- DE 0102798 W 20010723
- DE 10038728 A 20000731

Abstract (en)

[origin: US2003169629A1] A semiconductor memory cell configuration includes dynamic memory cells respectively having a trench capacitor and a vertical selection transistor, the memory cells being disposed in matrix form, the trench capacitors and the associated vertical selection transistors following one another in each case in the form of rows and/or columns.

IPC 1-7

H01L 21/8242

IPC 8 full level

H01L 21/8242 (2006.01); **H01L 27/108** (2006.01)

CPC (source: EP KR US)

H10B 12/00 (2023.02 - KR); **H10B 12/0383** (2023.02 - EP US)

Citation (search report)

See references of WO 0211200A1

Designated contracting state (EPC)

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DOCDB simple family (publication)

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