Title (en)

FAST SWITCHING INPUT BUFFER

Title (de)

SCHNELLSCHALTENDER EINGANGSPUFFER

Title (fr)

TAMPON D'ENTREE A COMMUTATION RAPIDE

Publication

EP 1307965 A1 20030507 (EN)

Application

EP 01950703 A 20010629

Priority

- US 0120818 W 20010629
- US 61635700 A 20000714

Abstract (en)

[origin: WO0207317A1] An input buffer circuit (300) for a semiconductor device that includes a PMOS transistor (306), an NMOS transistor (308), and a pull-up circuit (314). The pull-up circuit (314) applies a voltage to the bulk region of the PMOS transistor (306) causing a positive body effect which causes the absolute value of the voltage threshold of the PMOS transistor (306) to temporally lower when the input buffer (300) switches. This causes the input buffer (300) to switch faster than conventional input buffers. The input buffer (300) is an inverter, NOR, NAND, or other input buffer.

IPC 1-7

H03K 19/017

IPC 8 full level

H03K 19/0175 (2006.01); **H03K 19/017** (2006.01)

CPC (source: EP KR)

H03K 19/01707 (2013.01 - EP); **H03K 19/0175** (2013.01 - KR)

Citation (search report)

See references of WO 0207317A1

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DOCDB simple family (publication)

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US 0120818 W 20010629; AU 7167101 A 20010629; BR 0112513 A 20010629; CN 01812668 A 20010629; EP 01950703 A 20010629; JP 2002513098 A 20010629; KR 20037000515 A 20030113; TW 90116545 A 20010706