

Title (en)
SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD

Title (de)
HALBLEITERBAUELEMENT UND VERFAHREN ZU SEINER HERSTELLUNG

Title (fr)
DISPOSITIF A SEMI-CONDUCTEUR ET PROCEDE DE FABRICATION ASSOCIE

Publication
EP 1315212 A4 20080903 (EN)

Application
EP 01963539 A 20010907

Priority

- JP 0107810 W 20010907
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Abstract (en)
[origin: US2003020136A1] A DMOS device (or IGBT) includes an SiC substrate 2, an n-SiC layer 3 (drift region) formed in an epitaxial layer, a gate insulating film 6, a gate electrode 7a, a source electrode 7b formed to surround the gate electrode 7a, a drain electrode 7c formed on the lower surface of the SiC substrate 2, a p-SiC layer 4, an n+ SiC layer 3 formed to be present from under edges of the source electrode 7b to under associated edges of the gate electrode 7a. In addition, the device includes an n-type doped layer 10a containing a high concentration of nitrogen and an undoped layer 10b, which are stacked in a region in the surface portion of the epitaxial layer except the region where the n+ SiC layer 5 is formed. By utilizing a quantum effect, the device can have its on-resistance decreased, and can also have its breakdown voltage increased when in its off state.

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Citation (search report)

- [Y] DE 19900169 A1 19990708 - FUJI ELECTRIC CO LTD [JP]
- [Y] EP 0309290 A1 19890329 - NEC CORP [JP]
- [A] DE 19640561 A1 19970417 - SAMSUNG ELECTRONICS CO LTD [KR]
- See references of WO 0243157A1

Citation (examination)
TAKAHASHI K ET AL: "VERTICAL HOT-WALL TYPE CVD FOR SIC GROWTH", MATERIALS SCIENCE FORUM, AEDERMANNSTADT, CH, vol. 338-342, 1 January 2000 (2000-01-01), pages 141 - 144, XP008010071, ISSN: 0255-5476

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